CLAIMS

1. A method of measuring the resistance of a memory element comprising:

producing a plurality of electrical pulses at a rate related to said memory element resistance;

counting said electrical pulses over a predetermined time period to produce a pulse count; and

evaluating said pulse count to determine said resistance.

2. A method according to claim 1 wherein each said electrical pulse comprises a pulse of substantially uniform width.

3. A method according to claim 1 wherein said evaluating comprises comparing said pulse count to a reference pulse count to determine said memory element resistance.

4. A method according to claim 3 wherein said evaluating further comprises determining said memory element resistance as one value if said pulse count is above said reference pulse count and as another value if said pulse count is below said reference pulse count.

5. A method for sensing a resistance of a resistor comprising:

charging a capacitor to a voltage level;

discharging said capacitor through said resistor;

generating at least one recharging pulse each time the voltage on the capacitor falls below a predetermined value;

using said recharging pulse to recharge the voltage on said capacitor; and

determining said resistance from the number of recharging pulses which are generated during a predetermined period of time.

6. A method as defined in claim 5 wherein said discharging includes discharging said capacitor through said resistor at a substantially constant current.

7. A method of measuring a resistance of a resistor comprising:

applying a known voltage across said resistor such that a first current flows through said resistor;

withdrawing a current equal to said first current from a capacitor having a charge thereon;

replenishing said charge on said capacitor with a plurality of current pulses, such that one pulse of said plurality is applied to said capacitor when a voltage measured across said capacitor falls below a threshold voltage;

counting said plurality of pulses over a finite time period; and

determining a resistance of said resistor based on said counted pulses.

8. A method as in claim 7 further comprising comparing a value of counted pulses to a predetermined value to determine said resistance.

9. A method as in claim 8 wherein when a value of counted pulses is above a reference value, said resistance is determined as having one value and when a value of counted pulses is below said reference value said resistor is determined as having another value.

10. A method of measuring an impedance of a memory element comprising:

applying a substantially uniform voltage across said memory element;

flowing a substantially uniform current into said memory element from a charge reservoir;

flowing a plurality of current pulses into said charge reservoir;

controlling the flow of said plurality of current pulses in response to a quantity of charge in said charge reservoir;

counting said plurality of current pulses over a definite time to produce a pulse count; and

relating an impedance value of said memory element to said pulse count.

11. A method as defined in claim 10 wherein said impedance is an electrical resistance.

12. A method as defined in claim 10 wherein said impedance is a capacitance.

13. A method as defined in claim 10 wherein said impedance is an inductance.

14 . A memory integrated circuit comprising:

a capacitor;

a resistor;

a first circuit for conducting current from said capacitor through said resistor;

a controlled current source for delivering current to said capacitor;

a comparator for comparing a voltage on said capacitor to a reference voltage and supplying a pulse to turn on said current source when the voltage on said capacitor falls below said reference voltage;

a pulse counter operatively connected to said comparator output for counting pulses generated by said comparator; and

a second circuit for determining the value of said resistance based on the value stored in said pulse counter.

15. A memory integrated circuit as defined in claim 14 wherein said comparator further comprises a clock input, the output of said comparator changing state only when a clock signal applied to said clock input changes state.

16. A memory integrated circuit as defined in claim 14 wherein said second circuit is adapted to compare said value stored in said pulse counter to a reference value and determine whether said stored value is greater or less than said reference value.

17. A memory integrated circuit as defined in claim 14 wherein said first circuit further comprises:

a transistor having a source operatively connected to said capacitor, a gate, and a drain; and

a differential amplifier having a non-inverting input operatively connected to a first reference voltage, an output operatively connected to said gate, and an inverting input operatively connected to said drain and to said resistor.

18. A memory integrated circuit as defined in claim 14 wherein said second circuit further comprises a digital comparator adapted to receive said value stored in said pulse counter and to receive a reference value, and to compare said stored value to said reference value to produce an output.

19. A resistance measuring circuit comprising:

a capacitor having a first terminal;

a voltage controlled current source operatively connected to said first terminal, said current source adapted to withdraw current from said capacitor and supply said current to a resistor to be measured, said current source adapted to control said current according to a voltage measured across said resistor;

a current pulse generator having an output operatively connected to said first terminal, a clock input adapted to receive a periodic clock signal, and a voltage sensor, said pulse generator adapted to generate a current pulse synchronously with said clock signal

whenever said sensor indicates that a voltage at said first terminal is below a threshold voltage, whereby a plurality of current pulses are generated over time;

a first counter adapted to count cycles of said periodic clock signal to produce a clock count;

a second counter adapted to count pulses produced by said pulse generator to produce a pulse count; and

a circuit for determining a resistance value of said resistor in response to said pulse count and said clock count.

20. A resistance measuring circuit as in claim 19 wherein said voltage sensor further comprises a clocked comparator.

21. A resistance measuring circuit as in claim 19 wherein said current pulse generator further comprises a current source transistor having a source connected to a supply voltage, a gate, and a drain, a clocked comparator having an inverting input connected to said drain and to said first terminal, a non-inverting input connected to a reference voltage equal to said threshold voltage, an output connected to said gate, and a clock input adapted to receive said clock signal.

22. A resistance measuring circuit as in claim 19 wherein said circuit for determining resistance value further comprises a digital comparator adapted to compare

said pulse count to a reference count and produce a first output if said pulse count is above said reference count and a second output if said pulse count is below said reference count.

23. A memory storage device comprising:

a row line and a column line;

a memory cell including a cell resistor connected between said row line and said column line;

a control transistor having a first gate, a first terminal connected to said column line and a second terminal;

a switch for grounding said row line;

an amplifier having a first input connected to a first reference voltage source, a second input connected to said column line, and an output connected to said first gate;

a capacitor having a terminal connected to said second terminal of said control transistor;

a current supply transistor having a second gate, a first terminal connected to a power source, and a second terminal connected to said capacitor terminal;

a comparator having a first input connected to a second reference voltage source, and a second input connected to said capacitor terminal, said comparator having a pulse output which is connected to said second gate for turning on said current supply transistor when a voltage at said capacitor terminal falls below said second reference voltage; and

a circuit responsive to the output of said comparator for determining the resistance of said cell resistor.

24. A memory device as defined in claim 23, wherein said circuit comprises:

a first pulse counter having an input receiving a clock signal and a second pulse counter having an input receiving an output of said comparator, said circuit determining said resistance by determining the value held in said second counter when said first counter reaches a predetermined value.

25. A logic state sensor for a magnetic random access memory cell comprising:

a controlled voltage supply;

an electronic charge reservoir;

a current source;

a pulse counter;

said controlled voltage supply operatively connected to a resistive element of a magnetic random access memory device to maintain a substantially constant voltage across said resistive element;

said electronic charge reservoir operatively connected to said controlled voltage supply to provide a current through said resistive element;

said current source operatively connected to said charge reservoir to repeatedly supply a pulse of current to recharge said charge reservoir upon a predetermined depletion of electronic charge from said reservoir;

wherein said pulse counter count is a number of said pulses supplied by said current source over a predetermined time period, the contents of said pulse counter representing a logic state of said memory cell.

26. A processor system comprising:

a processor; and

a memory device coupled to said processor, said memory device including,

a row line and a column line;

a memory cell including a cell resistor connected between said row line and said column line;

a control transistor having a first gate, a first terminal connected to said column line and a second terminal;

a switch for grounding said row line;

an amplifier having a first input connected to a first reference voltage source, a second input connected to said column line, and an output connected to said first gate;

a capacitor having a terminal connected to said second terminal of said control transistor;

a current supply transistor having a second gate, a first terminal connected to a power source, and a second terminal connected to said capacitor terminal;

a comparator having a first input connected to a second reference voltage source, and a second input connected to said capacitor terminal, said comparator providing a pulse

output which is connected to said second gate for turning on said current supply transistor when a voltage at said capacitor terminal falls below said second reference voltage; and

a circuit responsive to the output of said comparator for determining the resistance of said cell resistor.

27. A processor system comprising:

a processor and a memory device coupled to said processor, said memory device including a memory cell logic state sensor, said sensor including a controlled voltage supply;

an electronic charge reservoir;

a current source;

a pulse counter;

said controlled voltage supply operatively connected to a resistive element of a magnetic random access memory device to maintain a substantially constant voltage across said resistive element;

said electronic charge reservoir operatively connected to said controlled voltage supply to provide a current through said resistive element;

said current source operatively connected to said charge reservoir to repeatedly supply a pulse of current to recharge said charge reservoir upon a predetermined depletion of electronic charge from said reservoir;

wherein said pulse counter count is a number of said pulses supplied by said current source over a predetermined time period, the contents of said pulse counter representing a logic state of said memory cell.